CPRE 4910 Weekly Report 03

10/7/2025 - 10/13/2025

Group number: SDMay26-24

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role:

Colin McGann	***-Project Lead***
Samuel Forde	***-PCB & Layout Lead***
Michael Drobot	***-Firmware Lead***
Jack Tonn	***-Testbench and Validation Lead***
Dawud Benedict	***-Toolflow Lead***
Emil Kosic	***-Repository and Coding Standards Lead***
Joshua Arceo	***-Client/Advisor Communications Lead***

- **Weekly Summary**

This week we started designing the ISA for our custom cores, optimized our rasterizer design, assembled the MemoryVGAPmod hardware, tested the hardware and memory controller, and worked on bringing up Cadence synthesis tools.

- **Past Week Accomplishments**
    - Colin McGann: Worked on the rasterization pipeline and testing the new memory hardware. Put together a Vivado project to quickly test all of our hardware. Also put together a simple VGA test.
    - Jack Tonn: Wrote a guide on how to use SVUnit testing framework, and how to initialize the framework to be able to build tests. Also modified project file structure to have a dedicated verification folder with all of the testbenches.
    - Dawud Benedict: Created an example on UVM with Questa. Started designing the Wishbone-to-PKBus bridge. Researched how to get Genus working with our PDK to get better timing, area, and power analysis from synthesis.

- Michael Drobot: Assembled and tested the MemoryVGAPmod hardware, started ChipForge digital design tutorials to prep for designing the VGA output module.
- Sam Forde: Put together vertex shading write-up, wrote some MAC units for testing, looking into performance comparison.
- Josh Arceo:
- Emil Kosic: Researched steps and minimum GPU core ISA instructions required for basic rendering.

- **Pending Issues**
  - We need a hardware test program to validate boards
  - Retroactively fitting Verilog testbenches into SVUnit

- **Individual contributions**

NAME	Individual Contributions	Hours this week	HOURS cumulative
Colin McGann	FPGA hardware testing system. Rasterization pipeline	15	55
Jack Tonn	SVUnit testing framework guide, continued to write test benches	6	26
Dawud Benedict	UVM example, WB-to-PKBus bridge design, Sky130 PDK with Cadence	6	20
Michael Drobot	MemoryVGAPmod assembly and test, ChipForge tutorials	10	22
Sam Forde	Vertex shading write-up	6	18
Josh Arceo	Looked into some ISA, finished chipforge tutorials for most part, watched CPRe 480 lectures	4	15
Emil Kosic	Gpu core ISA research and basic outline.chip forge ALU tutorial.	6	17

- **Comments and extended discussion**
  - None

- **Plans for the upcoming week**
  - Colin McGann: Continue work on optimization of the rasterizer and possibly move into other design components.
  - Jack Tonn: Go through verification flow again and teach it to others. Continue to update testbenches

- Dawud Benedict: Continue working on Genus setup with Sam. Continue and hopefully complete the WB-PK bridge. Learn SVUnit
- Michael Drobot:
- Sam Forde: Learn how to use verification flow.
- Josh Arceo: Start working on TB and learn verification.
- Emil Kosic: Continue Chipforge tutorials. Have a drawn out gpu core diagram with subcomponents with their inputs and outputs.